X(0) expected = 2 + j3

FPGA\_output R = 2 FPGA\_output I = 3

X(1) expected = 2.12 + j2.12

FPGA\_output R = 0 FPGA\_output I = -1

X(2) expected = 3 + j0

FPGA\_output R = 3 FPGA\_output I = 0

X(3) expected = 2.707 – j0.707

FPGA\_output R = -1 FPGA\_output I = -2

X(4) expected = 0 – j1

FPGA\_output R = 2.12 FPGA\_output I = 2.12

X(5) expected = -2.12 – j2.12

FPGA\_output R = -2.12 FPGA\_output I = -2.12

X(6) expected = -1 – j2

FPGA\_output R = 2.707 FPGA\_output I = -0.707

X(7) expected = 1.29 + j0.707

FPGA\_output R = 1.29 FPGA\_output I = 0.707